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UTILITY PATENT APPLICATION TRANSMITTAL

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APPLICATION ELEMENTS
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR LETTERS PATENT

Title : PLASMA DISPLAY DRIVING METHOD AND APPARATUS

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BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to an AC driving type plasma display driving method and apparatus.

[Description of the Related Art]

In recent years, plasma display panels (PDPs) have received a great deal of attention as a next-generation display device in place of CRTs because the PDPs are self-emission type display devices with good visibility, and can realize a low-profile large-screen display. In particular, an AC driving type PDP that can realize a large screen, is expected as a display device coping with high-quality digital broadcasting, and is demanded to attain higher image quality than the CRT.

Fig. 1 is a circuit diagram showing the whole arrangement of an AC driving type PDP apparatus. In Fig. 1, an AC driving type PDP 1 comprises scanning electrodes Y1 to Yn and common electrodes X parallel to each other on one surface, and address electrodes A1 to Am perpendicular to these electrodes Y1 to Yn and X on the opposing surface. The common electrodes X are laid out close to the scanning electrodes Y1 to Yn in correspondence with them, and have terminals commonly connected.

The common terminal of the common electrodes X is connected to the output terminal of an X driver 2, the scanning electrodes Y1 to Yn are connected to the

output terminals of a Y driver 3, and the address electrodes A1 to Am are connected to the output terminals of an address driver 4. The X driver 2, Y driver 3, and address driver 4 are controlled by control signals from a controller 5.

The controller 5 generates the control signals on the basis of external display data D, clock CLK indicating the read timing of the display data D, horizontal sync signal HS, and vertical sync signal VS, and supplies the control signals to the X driver 2, Y driver 3, and address driver 4.

Fig. 2 is a sectional view showing the structure of a cell Cij as one pixel on the i-th row and j-th column. In Fig. 2, a common electrode X and a scanning electrode Yi are formed on a front glass substrate 11. The common electrode X and scanning electrode Yi are covered with a dielectric layer 12 for insulating them from a discharge space 17, and the dielectric layer 12 is covered with a MgO (magnesium oxide) protective film 13.

An address electrode Aj is formed on a rear glass substrate 14 facing the front glass substrate 11, and covered with a phosphor 15. Ribs 16 for preventing color mixing between cells and maintaining a discharge gap are formed at pixel boundaries on the rear glass substrate 14 and address electrode Aj. Ne+Xe Penning gas is sealed in the discharge space 17 between the MgO protective film 13 and phosphor 15.

Fig. 3 is a voltage waveform chart showing an example of an AC driving type PDP driving method. Fig. 3 shows one of the subfields constituting one frame. Each subfield is divided into a reset period comprising a full-surface write period and full-surface erase period, address period, and sustain discharge period.

In the reset period, all scanning electrodes Y1 to Yn change to the ground level (0 V). At the same time, a full-surface write pulse of a voltage Vs+Vw (about 330 V) is applied to the common electrode X. At this time, all address electrodes A1 to Am are at a potential Vaw (about 100 V). As a result, all cells on all display lines discharge to generate wall charges regardless of the preceding display state.

The potentials of the common electrode X and address electrodes A1 to Am change to 0 V, and the voltages of wall charges themselves exceed the discharge start voltage in all cells to start discharging. During this discharge, since the electrodes do not have any potential difference, no wall charge is generated so that space charges self-neutralize to stop discharging. This is so-called self-erase discharge. This self-erase discharge makes all cells in the panel uniform freely from any wall charge. In this reset period, all cells can be made uniform regardless of the ON state of each cell in the preceding subfield. Thus, the

next address (write) discharge can be stably performed.

In the address period, address discharges are done line-sequentially in order to turn each cell on/off in accordance with display data. More specifically, a scan pulse of -Vy level (about -150 V) is applied to the scanning electrode Y1 corresponding to the first display line. At the same time, an address pulse of a voltage Va (about 50 V) is selectively applied to a cell that causes sustain discharge among the address electrodes A1 to Am, i.e., the address electrode Aj corresponding to a cell to be turned on.

Consequently, a discharge occurs between the address electrode Aj and scanning electrode Y1 of the cell to be turned on. Using this discharge as a priming effect (firing), the common electrode X of a voltage Vx (about 50 V) and scanning electrode Y1 immediately discharge. Then, a sufficient amount of wall charges for the next sustain discharge are accumulated in the MgO protective film 13 on the common electrode X and scanning electrode Y1 of the selected cell. The same processing is done for the scanning electrodes Y2 to Yn corresponding to the other display lines, and new display data are written in all display lines.

In the sustain discharge period, a sustain pulse of a voltage Vs (about 180 V) is alternately applied

to the scanning electrodes Y1 to Yn and common electrode X to perform sustain discharges so as to achieve a video display of one subfield. Note that the length of the sustain discharge period, i.e., the number of sustain pulses determine the video luminance.

In the above driving method, each subfield in one frame has the reset period, and a full-surface write discharge by application of the full-surface write pulse is done in each subfield. For this reason, each subfield emits light in the reset period not originally contributing to the video display, which decreases the video display contrast.

To solve this problem, the present applicant has invented and filed a driving method that realizes high contrast by decreasing the number of full-surface write discharges per frame (Japanese Patent Application Laid-Open No. 313598/1993). According to this driving method, the full-surface write discharge in the reset period is executed in only part of subfields in one frame, and only erase discharges in the reset period are executed in the remaining subfields.

In this high-contrast driving method, an erase discharge is performed in the reset period of the next subfield SFn+1 immediately after the sustain discharge (sustain) period of the n-th subfield SFn, as shown in Fig. 4. In this case, an erase pulse

made of a small-width pulse (e.g., a pulse width of 2 μs or less) is applied to the common electrode X to erase wall charges of each electrode only from the cell which was turned on in the preceding subfield SFn.

An allowable range (voltage range from the minimum value to the maximum value will be called a driving voltage margin) is defined for the voltage values of various pulses for realizing driving of normally turning an ON cell on based on display data while keeping an OFF cell off. If the discharge starts unexpectedly early owing to nonuniform pixels and temperature condition changes in the small-width erase discharge during the reset period, a necessary wall charge erase fails. In addition, wall charges opposite in polarity to wall charges before an erase may be generated on the common electrode X and scanning electrode Y. This narrows the driving voltage margin.

To solve this problem, the present applicant has further invented and filed a new driving method (US Patent Application Serial No. 115911 filed on July 15, 1998). According to this driving method, after a small-width pulse is applied during the reset period, another erase pulse (Slope Erase Pulse: SEP) which rises with a gradual slope is applied to make an erroneous erase state come close to a more complete erase state.

Fig. 5 shows an example of this driving method. Fig. 5 is a driving waveform chart showing part of the reset period in a given subfield. In an ON cell in which the final sustain discharge was done in a preceding subfield, positive and negative charges are respectively accumulated in the common electrode X and scanning electrode Y. In this state, an erase pulse of the voltage Vs made of a small-width pulse is applied to the common electrode X to erase wall charges of the ON cell, as shown in Fig. 5.

Note that the small-width pulse terminates application of the pulse voltage immediately after a discharge. Most of charge particles generated by the discharge are left in the discharge cell space, attracted by an electrostatic attraction to wall charges of the dielectric layer of the panel, and recombine each other and disappear on the wall surface. Such a strong discharge using a rectangular wave, however, may generate new wall charges opposite in polarity to wall charges before an erase, in the common electrode X and scanning electrode Y, as described above.

To prevent this, after an erase discharge using the small-width pulse is performed, an erase pulse (to be referred to as a positive obtuse wave) which rises to the voltage Vs with a gradual slope and an erase pulse (to be referred to as a negative obtuse wave) which falls to a voltage -Vy with a gradual

slope are sequentially applied. Wall charges having an inverted polarity which are left owing to an excessive reaction with the small-width pulse, and wall charges which cannot completely be erased by the erase discharge using the small-width pulse are reacted and erased with the potentials of the positive and negative obtuse waves which gradually change with time.

More specifically, the amount of wall charges accumulated in a cell which was turned on in the preceding subfield is not always the same in all cells, so the discharge start voltage of each cell varies. If such obtuse waves are applied in this state, discharges sequentially occur from cells in which the pulse voltage during the rise of the positive obtuse wave and the fall of the negative obtuse wave reaches the discharge voltage. Each cell substantially receives the optimum voltage (voltage almost equal to the discharge start voltage). This can erase the residual charges.

In this related art, however, the erase discharge is done only for the cell, which was turned on in the preceding subfield among subfields except for a specific subfield in the high-contrast driving method. Under the influence of wall charges accumulated in the ON cell, charges may be accumulated in an OFF cell, which has been kept off, may not be erased, and may be left. Figs. 6A to 6C are representations for

respectively illustrating the states of charges accumulated in the OFF cell.

As shown in Fig. 6A, in an ON cell in which the final sustain discharge was done in the preceding subfield, positive charges are accumulated in its address electrode A and common electrode X, and negative charges are accumulated in its scanning electrode Y. Even in an OFF cell adjacent to the ON cell, weak positive wall charges are accumulated in its address electrode A and scanning electrode Y of the OFF cell, and weak negative wall charges are accumulated in its common electrode X under the influence of the wall charges accumulated in the ON cell.

If an erase discharge using the small-width pulse is executed in this state during the reset period of the next subfield, new wall charges opposite in polarity to the wall charges before being erased may be generated on the common electrode X and scanning electrode Y, as shown in Fig. 6B. If the erase discharge using the obtuse wave as shown in Fig. 5 is executed, wall charges accumulated in the ON cell are erased to be free from any residual charges, as shown in Fig. 6C.

The ON cell accumulates charges enough for satisfactorily starting discharging by the pulse voltage during the rise of the positive obtuse wave and the fall of the negative obtuse wave. By

applying these positive and negative obtuse waves, the discharge can occur to erase residual charges. In the OFF cell, however, wall charges accumulated under the influence of the adjacent ON cell are weak. Even if the pulse voltage of the obtuse wave changes to the voltage Vs or -Vy, the OFF cell cannot reach the discharge start voltage, so wall charges cannot be erased and are left.

In this case, if the cell is kept off for several frames, like a still image and the background of a moving picture, the amount of residual charges accumulated in the OFF cell increases gradually. If a sufficient amount of residual charges, which cannot react with respect to the positive and negative obtuse waves, is accumulated in the OFF cell, the OFF cell which should not be turned on is turned on under the influence of residual charges to narrow the driving voltage margin.

Fig. 7 is a representation for illustrating this conventional problem. As shown in Fig. 7, a scan pulse of -Vy level is applied to scanning electrodes Yi and Yi+2 of cells C1 and C3 to be turned on in accordance with display data. At the same time, an address pulse of Va level is selectively applied to an address electrode A corresponding to the cells to be turned on, so as to emit light from the cells.

But, if a sufficient amount of residual charges is accumulated in an OFF cell C2 not to be turned on,

an address pulse is applied owing to positive charges on the address electrode A to operate the cell C2 as if a scan pulse is applied owing to negative charges on a scanning electrode Yi+1. This causes a miss discharge in the OFF cell to generate wall charges. A sustain discharge is undesirably done in the OFF cell during the subsequent sustain discharge period to turn on the OFF cell though it should not be turned on.

SUMMARY OF THE INVENTION

The present invention has been made to overcome the conventional drawbacks, and aims to improve the driving voltage margin in driving a PDP, and reliably to realize driving of normally turning on an ON cell that should be turned on based on display data while keeping an OFF cell off.

To achieve the above object, in a plasma display driving method according to the present invention, each frame comprises subfields; each of the subfields includes a reset period for performing an erase discharge to make a wall charge distribution in each cell uniform, an address period for generating wall charges in a cell to be turned on in accordance with display data, and a sustain discharge period for discharging the wall charges accumulated in the cell during the address period, to emit light; and the reset period includes first and second erase discharge periods for performing erase discharges for

cells having been turned on and not having been turned on, respectively.

The present invention can apply to a so-called high-contrast driving method. In this case, erase discharges done separately in the first and second erase discharge periods are executed in subfields except for a specific subfield.

A plasma display driving apparatus according to the present invention is for driving a plasma display panel in each of the subfields constituting one frame. Each of the subfields includes a reset period for performing an erase discharge to make a wall charge distribution in each cell uniform, an address period for generating wall charges in a cell to be turned on in accordance with display data, and a sustain discharge period for discharging the wall charges accumulated in the cell during the address period, to emit light. The apparatus comprises control means for performing erase discharges for cells having been turned on and not having been turned on, in first and second erase discharge periods in the reset period, respectively.

According to the present invention having the above features, during the reset period after the sustain discharge period, an erase discharge is done in the first erase discharge period for an ON cell turned on in the preceding sustain discharge period, so as to erase wall charges in the ON cell, for

example. Even for an OFF cell not turned on in the preceding sustain discharge period, an erase discharge is done in the second erase discharge period on the basis of a pulse voltage having a different waveform from that for the ON cell. As a result, even weak wall charges accumulated in the OFF cell under the influence of the ON cell can be erased.

For example, the erase discharge for the OFF cell is achieved by applying to the first electrode the first erase pulse whose application voltage continuously changes with time in a positive direction, and applying to the second electrode the second erase pulse whose application voltage continuously changes with time in a negative direction. This can widen the potential difference between the first and second electrodes to erase even weak wall charges accumulated in the OFF cell under the influence of the ON cell.

In other words, the present invention performs erase discharges for ON and OFF cells in the first and second erase discharge periods in the reset period, respectively. Weak wall charges that could not completely be erased in the first erase discharge period, i.e., weak wall charges accumulated in the OFF cell under the influence of the ON cell can be erased in the second erase discharge period. This makes it possible to prevent an ON operation of the OFF cell that should not be turned on in the

subsequent address period and sustain discharge period, and to improve the driving voltage margin.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing the whole arrangement of an AC driving type plasma display panel apparatus;

Fig. 2 is a sectional view showing the structure of a cell Cij as one pixel on the i-th row and j-th column;

Fig. 3 is a waveform chart showing an example of a conventional AC driving type PDP driving method;

Fig. 4 is a representation of the structure of a subfield for use in explaining the conventional AC driving type PDP driving method;

Fig. 5 is a waveform chart showing an example of the AC driving type PDP driving method;

Figs. 6A to 6C are representations for illustrating the respective states of wall charges accumulated in electrodes at the end of a sustain discharge and during a reset period when the AC driving type PDP driving method of Fig. 5 is applied, in which Fig. 6A shows the state at the end of a sustain discharge of the preceding subfield, Fig. 6B shows the state in the reset period of the next subfield, and Fig. 6C shows the state after an erase discharge;

Fig. 7 is a representation for illustrating problems when the AC driving type PDP driving method

of Fig. 5 is applied;

Fig. 8 is a representation of the structure of a subfield for use in explaining an AC driving type PDP driving method according to an embodiment of the present invention;

Fig. 9 is a waveform chart showing an example of driving waveform in an AC driving type PDP according to the embodiment;

Figs. 10A and 10B are waveform charts each showing a variable ultimate voltage Vax of a second positive obtuse wave;

Fig. 11 is a circuit diagram showing an example of hardware arrangement for realizing the variable ultimate voltage Vax of the second positive obtuse wave;

Figs. 12A to 12D are representations for illustrating the respective states of wall charges accumulated in electrodes when the AC driving type PDP driving method according to the embodiment is applied, in which Fig. 12A shows the state at the end of a sustain discharge of the preceding subfield, Fig. 12B shows the state in the reset period of the next subfield, Fig. 12C shows the state in the first erase discharge period, and Fig. 12D shows the state in the second erase discharge period;

Fig. 13 is a waveform chart showing another example of driving waveform of the AC driving type PDP according to the embodiment; and

Fig. 14 is a timing chart showing another example of rise timing of the second positive obtuse wave applied in the embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described below with reference to the accompanying drawings.

In this embodiment, the present invention applies to a high-contrast driving method. In subfields except for a specific subfield (e.g., the first subfield in each frame), an erase discharge is only done in the reset period without performing any full-surface write discharge.

Figs. 1 and 2 show the whole arrangement of an AC driving type PDP apparatus and the sectional structure of one cell according to this embodiment, respectively. Control means according to the present invention comprises a controller 5 in Fig. 1. Fig. 8 is a representation of the structure of a subfield for used in explaining a PDP driving method according to this embodiment.

In this embodiment, each subfield is divided into a reset period, an address period, and a sustain discharge (sustain) period. The reset period is further divided into the first erase discharge period in which an erase discharge is done for the cell which was turned on in the sustain discharge period of a preceding subfield, and the second erase

discharge period in which an erase discharge of wall charges accumulated in an OFF cell under the influence of an adjacent ON cell is done even for the cell which was not turned on in the sustain discharge period of the preceding subfield.

In the first and second erase discharge periods, the residual charges in the ON and OFF cells are respectively erased by different application waveforms. In the first erase discharge period, a small-width pulse is applied to a common electrode X, and then an erase pulse (to be referred to as the first positive obtuse wave) which gradually rises to a voltage Vs with a gradual slope is applied to a scanning electrode Y. Wall charges accumulated in the ON cell by a sustain discharge in the preceding subfield are thereby erased by an erase discharge.

In the second erase discharge period, an erase pulse (corresponding to the first erase pulse in the present invention; to be referred to as the second positive obtuse wave) which gradually rises to a voltage Vax with a gradual slope is applied to the common electrode X (first electrode in the present invention). In addition, an erase pulse (corresponding to the second erase pulse in the present invention; to be referred to as a negative obtuse wave) which gradually falls to a voltage -Vy with a gradual slope is applied to the scanning electrode Y (second electrode in the present

invention). As a result, wall charges left in the OFF cell under the influence of an adjacent ON cell are erased by an erase discharge.

Fig. 9 is a waveform chart showing an example of the driving waveform of the AC driving type PDP according to this embodiment, and shows one subfield except for a specific subfield in the high-contrast driving method.

As described above, in the first erase discharge period, the scanning electrode Y changes to ground level (0 V). At the same time, a small-width pulse of the voltage Vs (about 180 V) is applied to the common electrode X to erase wall charges in the ON cell. After the erase discharge using this small-width pulse, the first positive obtuse wave which gradually rises to the voltage Vs with a gradual slope is applied to the scanning electrode Y to erase wall charges having an inverted polarity which are left owing to an excessive reaction with the small-width pulse, and wall charges which cannot completely be erased by the erase discharge using the small-width pulse.

In the second erase discharge period, the negative obtuse wave which gradually falls to the voltage -Vy (about -150 V) with a gradual slope is applied to the scanning electrode Y. At the same time, the second positive obtuse wave, which gradually rises to the voltage Vax with a gradual

slope, is applied to the common electrode X. By applying the second positive obtuse wave to the common electrode X in synchronism with application of the negative obtuse wave to the scanning electrode Y, the voltage difference between the electrodes X and Y can be widened to erase even weak wall charges left in the OFF cell by the erase discharge.

In this manner, the residual charges in the OFF cell can be erased before the address period. When an address pulse is selectively applied to an address electrode A on the basis of display data in the subsequent address period, and a scan pulse is applied to the scanning electrode Y to perform address discharges line-sequentially, any miss discharge on the OFF cell can be prevented. Consequently, in the subsequent sustain discharge period, the OFF cell which should not be turned on can be prevented from being turned on by the sustain discharge in the OFF cell.

The application timing of the second positive obtuse wave is the same as the application timing of the negative obtuse wave, for example. The pulse widths (rise time and fall time) of the second positive obtuse wave and negative obtuse wave have time widths enough for satisfactorily reaching the ultimate voltages Vax and -Vy at the resistances of circuits for generating these obtuse waves. If the slope of the obtuse wave is steep, the executed erase

discharge may become strong. To prevent this, the resistance values of the circuits for generating the second positive obtuse wave and negative obtuse wave are respectively set so as to change these obtuse waves gradually. To allow each obtuse wave to reach a necessary voltage even at such resistances, the rise/fall time is set to, e.g., 100 μsec or more.

The final ultimate voltage Vax of the second positive obtuse wave is set such that the potential difference from the ultimate voltage -Vy of the negative obtuse wave is around the discharge start voltage (voltage at which a discharge occurs regardless of the presence/absence of wall charges) between the electrodes X and Y and is lower than this discharge start voltage. This is because a full discharge occurs if the voltage difference between the electrodes X and Y is equal to or larger than the discharge start voltage.

The potential difference between the ultimate voltage Vax of the second positive obtuse wave applied to the common electrode X and the ultimate voltage -Vy of the negative obtuse wave applied to the scanning voltage Y is adjusted around the discharge start voltage. For this purpose, this embodiment can increase/decrease the value of the ultimate voltage Vax of the second positive obtuse wave, as shown in Figs. 10A and 10B. Fig. 11 shows an example of an arrangement for attaining the

purpose. Fig. 11 shows part of the AC driving type PDP apparatus shown in Fig. 1, and shows voltage setting means of the present invention.

In Fig. 11, a positive obtuse wave generator 21 is for generating the second positive obtuse wave. A negative obtuse wave generator 22 is for generating the negative obtuse wave. The positive and negative obtuse wave generators 21 and 22 are respectively incorporated in the X driver 2 and Y driver 3 shown in Fig. 1. The positive and negative obtuse wave generators 21 and 22 are connected to the common electrode X and scanning electrode Y of the AC driving type PDP 1, respectively.

The positive obtuse wave generator 21 comprises a resistor 23 for determining the rise slope of the second positive obtuse wave. The negative obtuse wave generator 22 comprises a resistor 24 for determining the fall slope of the negative obtuse wave. In this embodiment, the resistor 23 for the second positive obtuse wave is variable so as to increase/decrease a resistance value Rx and increase/decrease the value of the ultimate voltage Vax of the second positive obtuse wave. Note that the resistor 24 in the negative obtuse wave generator 22 may also be variable so as to increase/decrease a resistance value Ry.

The negative obtuse wave and second positive obtuse wave have the same application start timing,

whereas the resistance values Rx and Ry cannot take the same value because of different final ultimate voltages. If the second positive obtuse wave rises too steeply, residual charges excessively react; if the second positive obtuse wave rises too slowly, the wave does not reach a desired voltage. Considering them, the resistance value Rx for the second positive obtuse wave must be optimized.

Figs. 12A to 12D are representations for illustrating the respective states of wall charges accumulated in the address electrode A, common electrode X, and scanning electrode Y when the PDP driving method according to this embodiment is applied. The charge accumulation states shown in Figs. 12A to 12C correspond to the states shown in Figs. 6A to 6C, respectively. That is, wall charges accumulated in the ON cell at the end of the sustain discharge period are erased by applying the small-width pulse and first positive obtuse wave in the first erase discharge period, and applying the negative obtuse wave in the second erase discharge period.

In addition, in this embodiment, the second positive obtuse wave is applied in synchronism with application of the negative obtuse wave in the second erase discharge period, so as to erase even weak residual charges accumulated in the OFF cell under the influence of the ON cell, as shown in Fig. 12D.

This can prevent an ON operation of the OFF cell that should not be turned on in the subsequent address period and sustain discharge period, and can improve the driving voltage margin.

In the above embodiment, an obtuse wave whose change rate per unit time gradually changes is applied as an erase pulse whose application voltage gradually changes with time, to the common electrode X and scanning electrode Y in the reset period. But, the present invention is not limited to this. For example, a triangular wave whose application voltage gradually changes at a constant change rate per unit time may be applied, as shown in Fig. 13.

In this embodiment, the rise start timing of the second positive obtuse wave and the fall start timing of the negative obtuse wave are synchronized. But, the present invention is not limited to this. For example, the rise start timing of the second positive obtuse wave applied to the common electrode X may be delayed from the fall start timing of the negative obtuse wave applied to the scanning electrode Y, so as to narrow the pulse width of the second positive obtuse wave, as shown in Fig. 14.

In this embodiment, the positive obtuse wave that rises in a positive direction is applied as an obtuse wave applied to the common electrode X in synchronism with the negative obtuse wave to the scanning electrode Y. Alternatively, a negative obtuse wave

that falls in a negative direction may be applied to the common electrode X in synchronism with the first positive obtuse wave to the scanning electrode Y. But, the alternative method can be taken only when a time margin (e.g., an interval of 10 μsec or more) is set between the fall of the small-width pulse and application of the negative obtuse wave. This is because an erase may undesirably be done in an unstable charge state if the interval between the small-width pulse and negative obtuse wave is less than 10 μsec.

This embodiment has exemplified the high-contrast driving method. That is, a full-surface write and full-surface erase are performed during the reset period in the first subfield of each frame, and the above-described driving method is executed in the second and subsequent subfields. But, the principle of this embodiment is not limited to the high-contrast driving method.

For example, when full-surface write/small-width erase discharges are executed in the reset periods of all subfields, the same driving method as in this embodiment can apply to each of the subfields to produce the same effects as in the embodiment. Even when small-width erase discharges are done in the reset periods of all subfields without performing full-surface write discharges, the present invention is effective.

WHAT IS CLAIMED IS:

1. A plasma display driving method wherein each frame comprises subfields; each of said subfields includes a reset period for performing an erase discharge to initialize a wall charge distribution in each cell, an address period for generating a wall charge distribution in accordance with display data, and a sustain discharge period for discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light; and

said reset period includes first and second erase discharge periods for performing erase discharges for cells having been turned on and not having been turned on, respectively.

2. A method according to claim 1, wherein a full-surface write discharge and a full-surface erase discharge are done during said reset period only in a specific subfield among the subfields in each frame, erase discharges for erasing wall charges accumulated in cells are done during said reset periods in the remaining subfields without performing said full-surface write discharges, and the erase discharges done separately in said first and second erase discharge periods are executed in the subfields except for said specific subfield.

3. A method according to claim 1, wherein the erase discharge in each said second erase discharge

period is achieved by applying to a first electrode a first erase pulse whose application voltage continuously changes with time in a positive direction, and applying to a second electrode a second erase pulse whose application voltage continuously changes with time in a negative direction.

4. A method according to claim 3, wherein the pulse widths of said first and second erase pulses have time widths required to reach the ultimate voltages of said first and second erase pulses.

5. A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates per unit time of the application voltage change with time.

6. A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates per unit time of the application voltage are constant.

7. A method according to claim 3, wherein the potential difference between the ultimate voltages of said first and second erase pulses is around the discharge start voltage between said first and second electrodes and is smaller than said discharge start voltage.

8. A method according to claim 7, wherein at least one of said ultimate voltages of said first and second erase pulses is variable.

9. A method according to claim 3, wherein the rise start timing of said first erase pulse is synchronized with or delayed from the fall start timing of said second erase pulse.

10. A plasma display driving apparatus for driving a plasma display panel in each of the subfields constituting one frame, each of said subfields including a reset period for performing an erase discharge to initialize a wall charge distribution in each cell, an address period for generating a wall charge distribution in accordance with display data, and a sustain discharge period for discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light, said apparatus comprising:

a controller for performing erase discharges for cells having been turned on and not having been turned on, in first and second erase discharge periods in said reset period, respectively.

11. An apparatus according to claim 10, wherein said controller performs a full-surface write discharge and a full-surface erase discharges during said reset period only in a specific subfield among the subfields in each frame, erase discharges for erasing wall charges accumulated in cells during said reset periods in the remaining subfields without performing said full-surface write discharges, and

executes the erase discharges done separately in said first and second erase discharge periods in the subfields except for said specific subfield.

12. An apparatus according to claim 10, wherein said controller performs the erase discharge for an OFF cell in each said second erase discharge period by applying to a first electrode a first erase pulse whose application voltage continuously changes with time in a positive direction, and applying to a second electrode a second erase pulse whose application voltage continuously changes with time in a negative direction.

13. An apparatus according to claim 12, wherein said controller applies, as said first and second erase pulses, pulse voltages having waveforms whose change rates per unit time of the application voltage change with time.

14. An apparatus according to claim 12, further comprising voltage setting unit for setting the potential difference between the ultimate voltages of said first and second erase pulses to be around the discharge start voltage between said first and second electrodes and to be smaller than said discharge start voltage.

15. An apparatus according to claim 14, wherein said voltage setting unit can change at least one of the ultimate voltages of said first and second erase pulses.

16. An apparatus according to claim 15, wherein said voltage setting unit comprises a first resistor in a pulse generation circuit for generating said first erase pulse and a second resistor in a pulse generation circuit for generating said second erase pulse, and at least one of said first and second resistors is variable.

17. An apparatus according to claim 16, wherein said first and second resistors have different resistance values.

18. An apparatus according to claim 12, wherein said controller synchronizes or delays the rise start timing of said first erase pulse with or from the fall start timing of said second erase pulse.

ABSTRACT OF THE DISCLOSURE

In a reset period after a sustain discharge period, erase discharges are done by applying pulse voltages having different waveforms in the first erase discharge period for an ON cell turned on in the preceding sustain discharge period and in the second erase discharge period even for an OFF cell not turned on in the preceding sustain discharge period. Weak wall charges that could not completely be erased in the first erase discharge period, i.e., weak wall charges having been accumulated in the OFF cell under the influence of the ON cell can be erased in the second erase discharge period. This makes it possible to prevent an ON operation of the OFF cell that should not be turned on in the subsequent address period and sustain discharge period, and to improve the driving voltage margin.

FIG. 1

AC DRIVING TYPE PLASMA DISPLAY APPARATUS

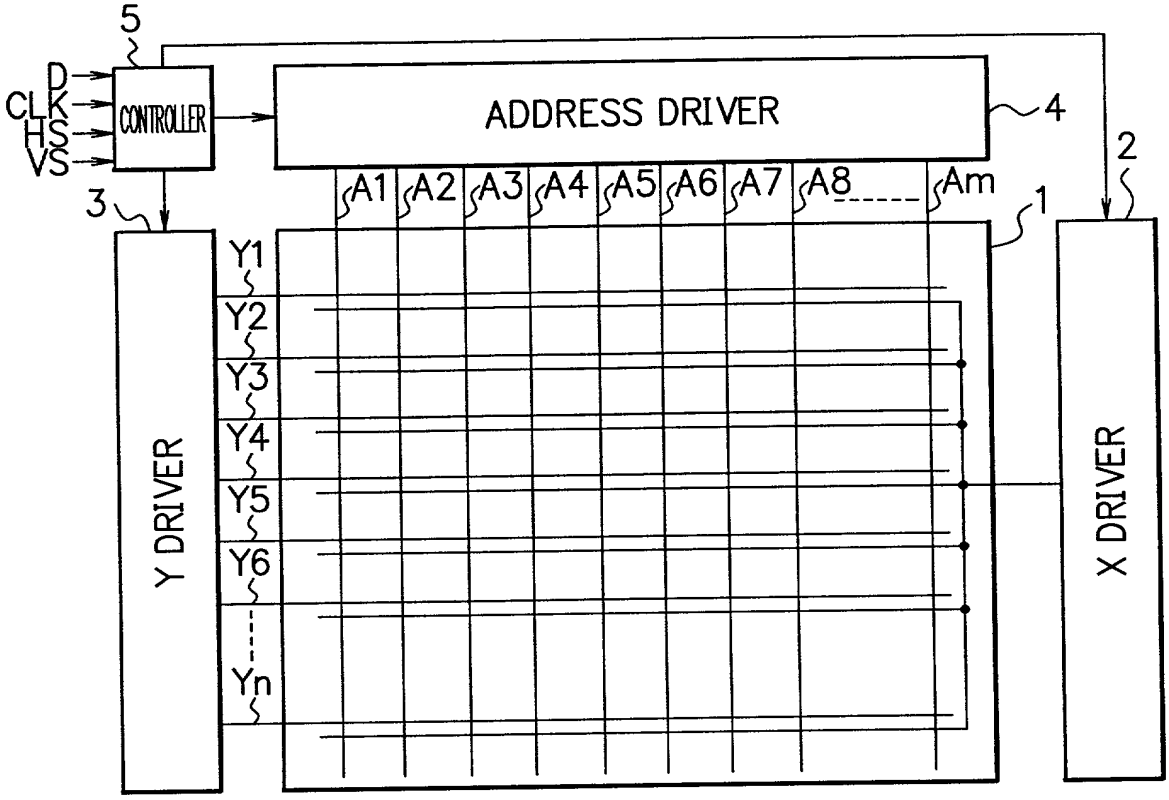


FIG. 2

SECTIONAL STRUCTURE OF CELL

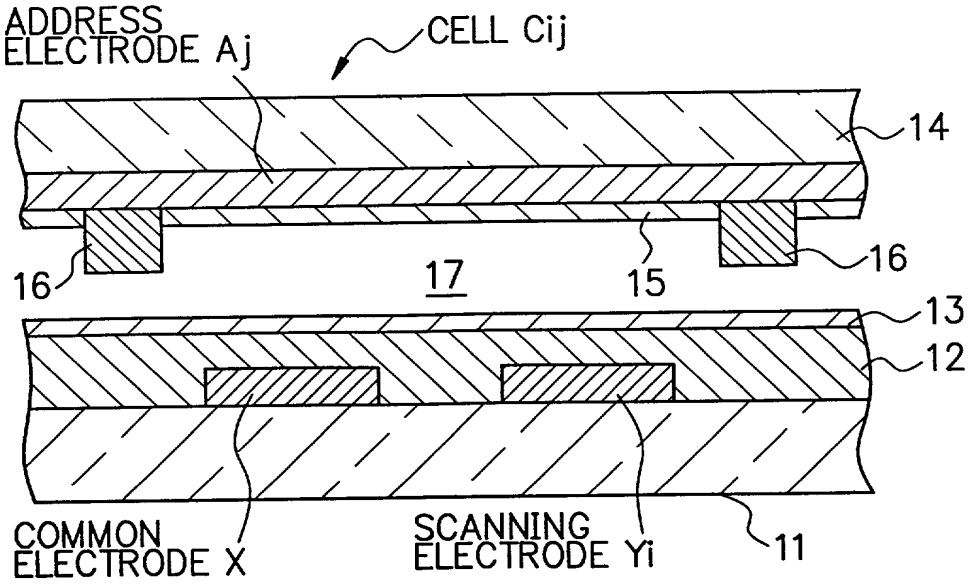


FIG. 3 WAVEFORM CHART SHOWING CONVENTIONAL DRIVING METHOD

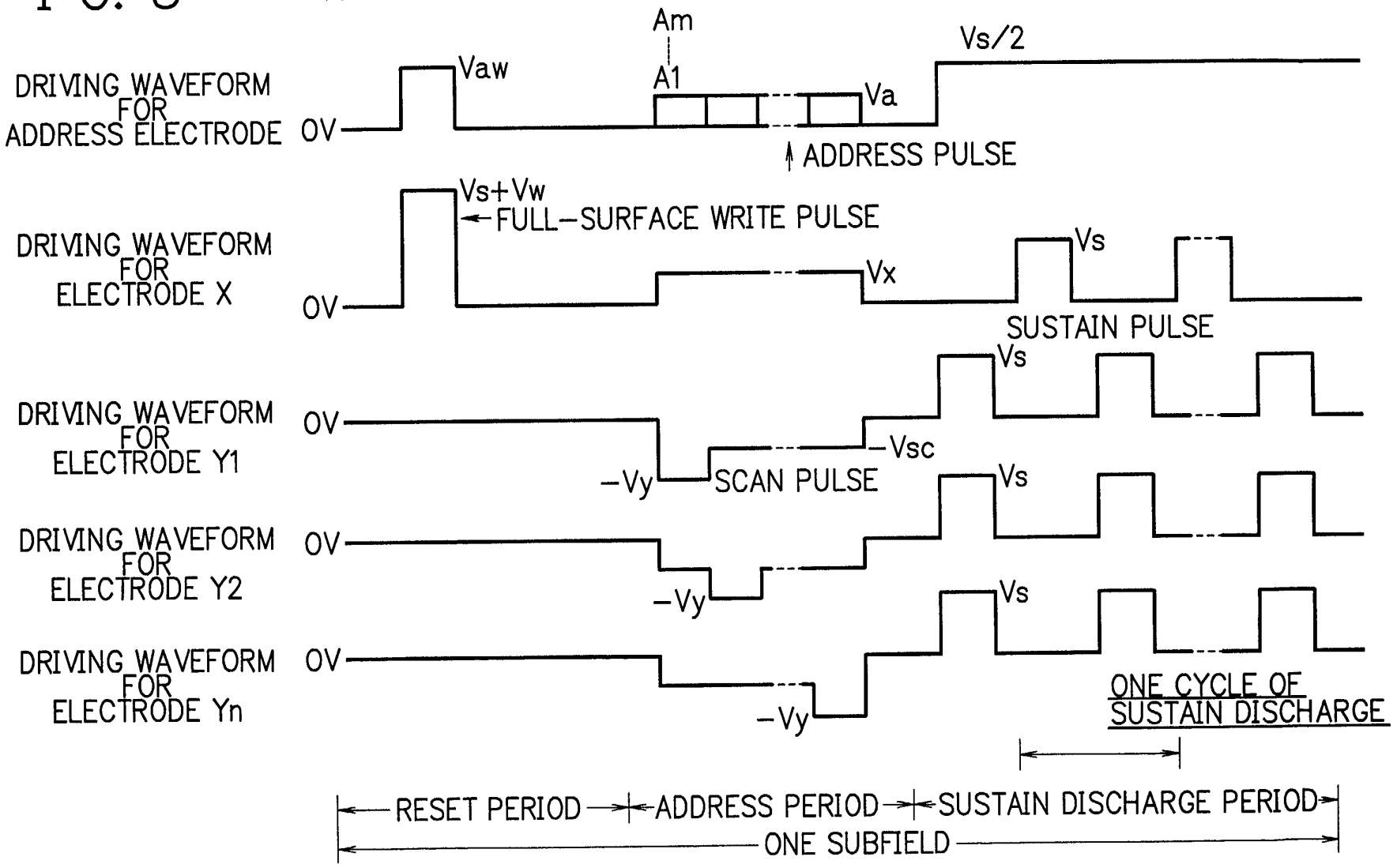


FIG. 4

CONVENTIONAL SUBFIELD STRUCTURE

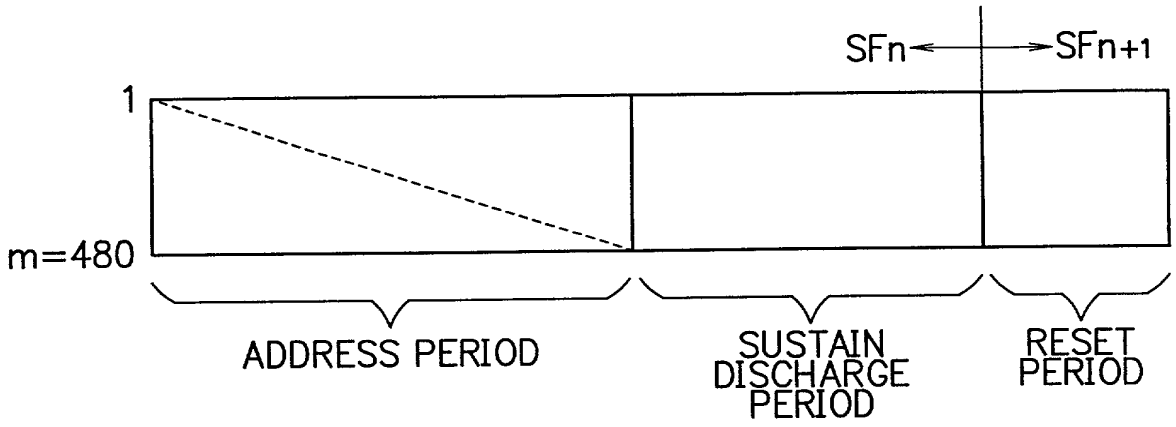
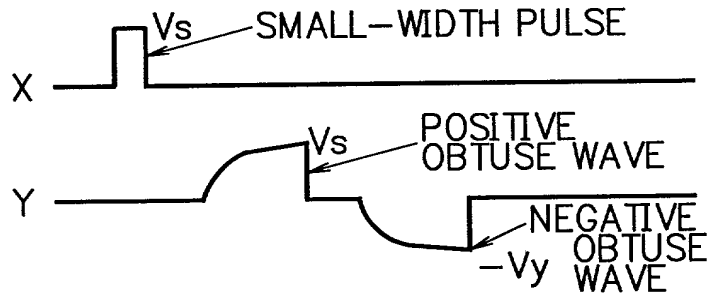


FIG. 5

WAVEFORM CHART SHOWING EXAMPLE OF PDP DRIVING METHOD



CHARGE ACCUMULATION STATE

FIG. 6A

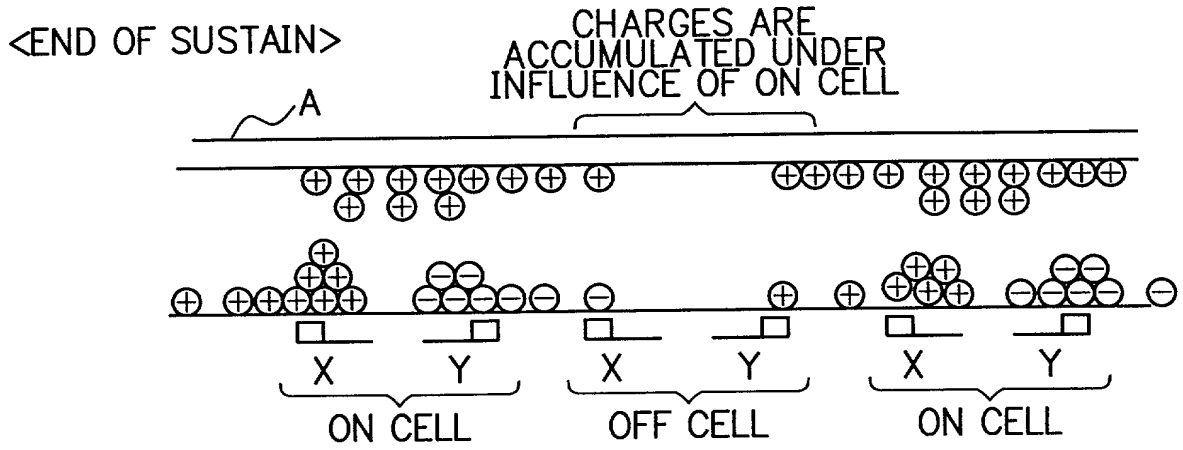


FIG. 6B

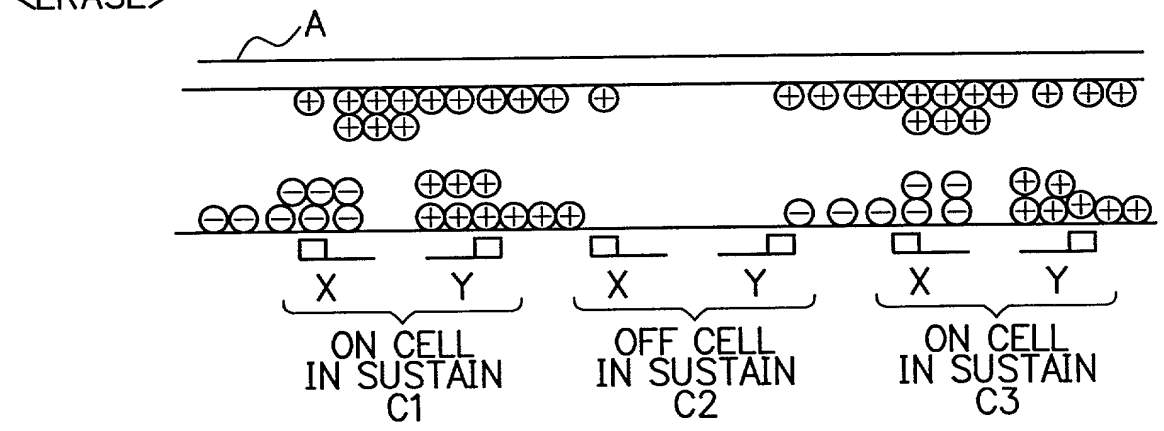


FIG. 6C

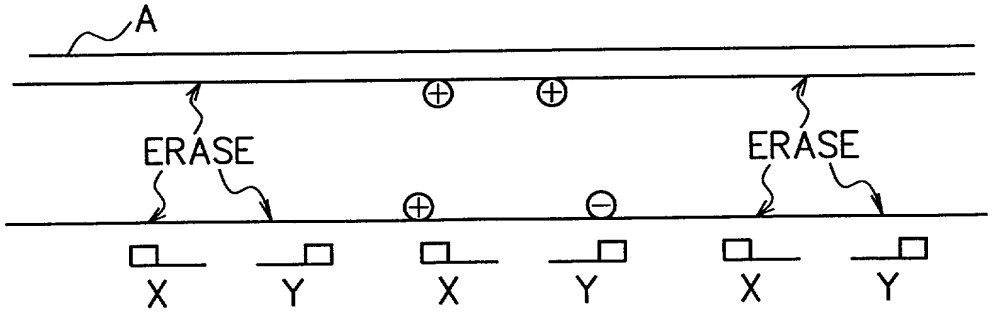


FIG. 7

CHARGE ACCUMULATION STATE IN ADDRESS PERIOD

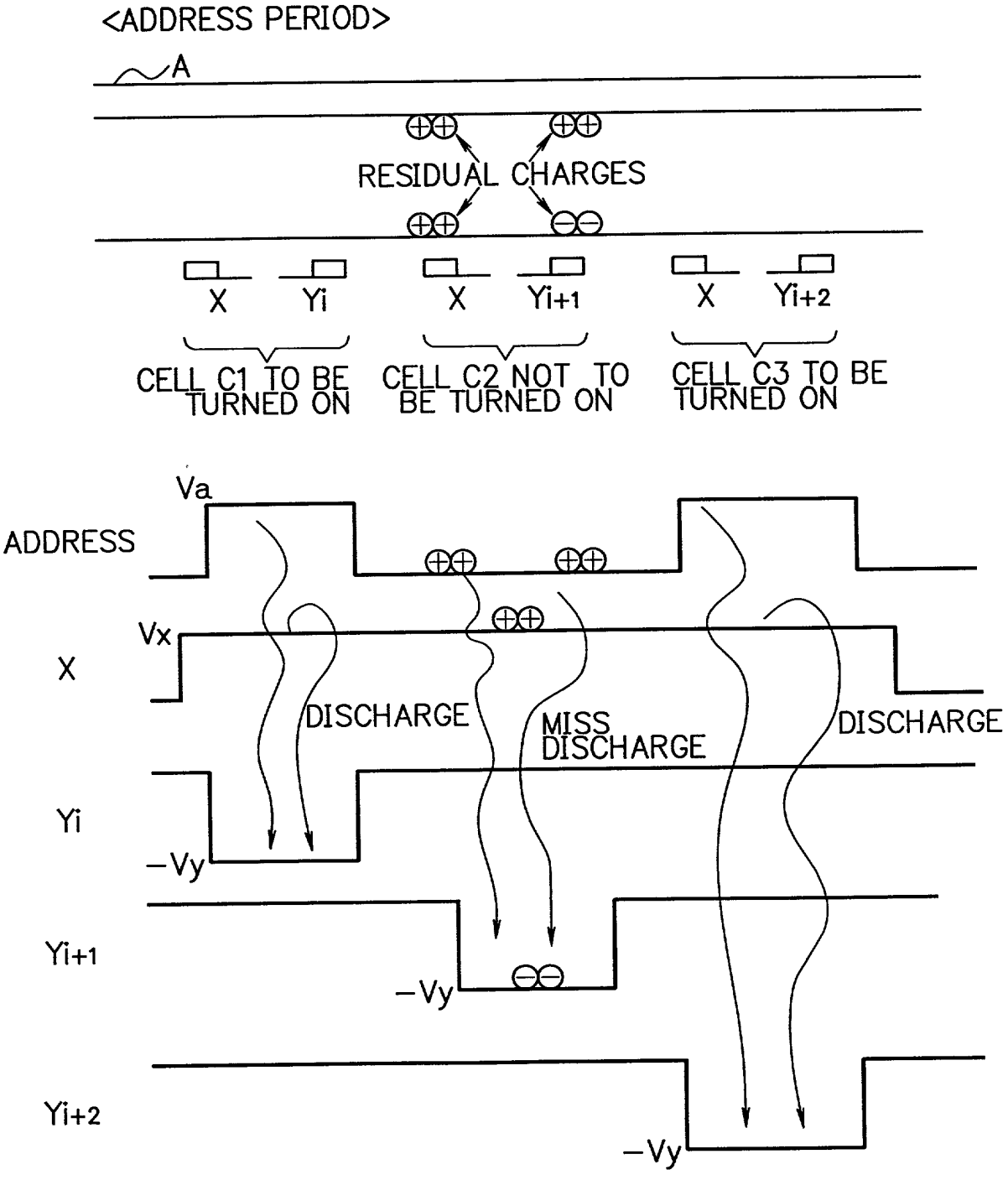


FIG. 8

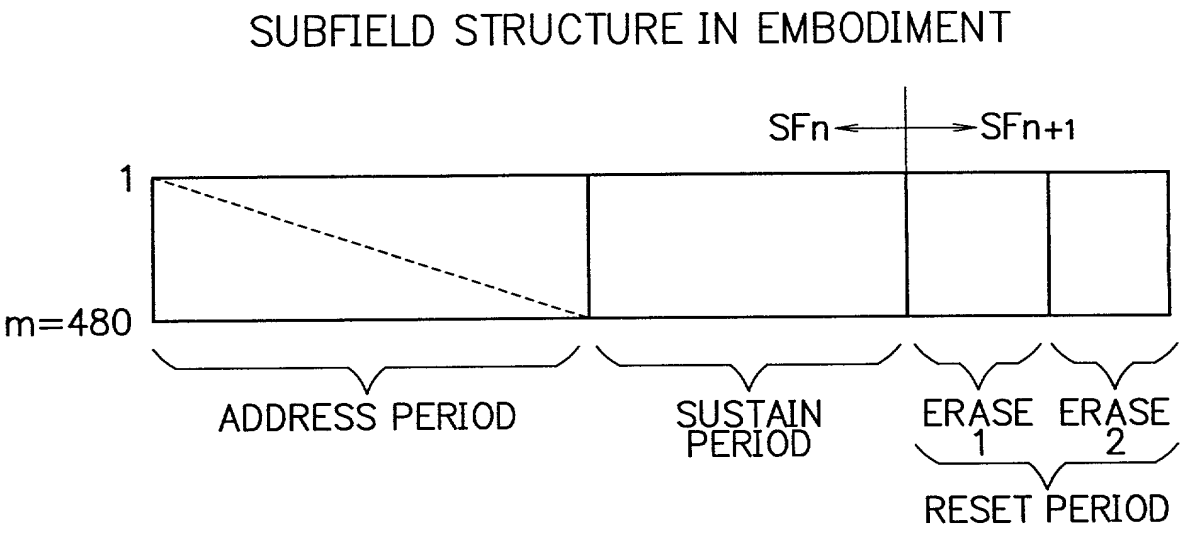

SUBFIELD STRUCTURE IN EMBODIMENT
SFn
SFn+1
1
m=480
ADDRESS PERIOD
SUSTAIN PERIOD
ERASE 1
ERASE 2
RESET PERIOD

FIG. 9

PDP DRIVING WAVEFORM IN EMBODIMENT

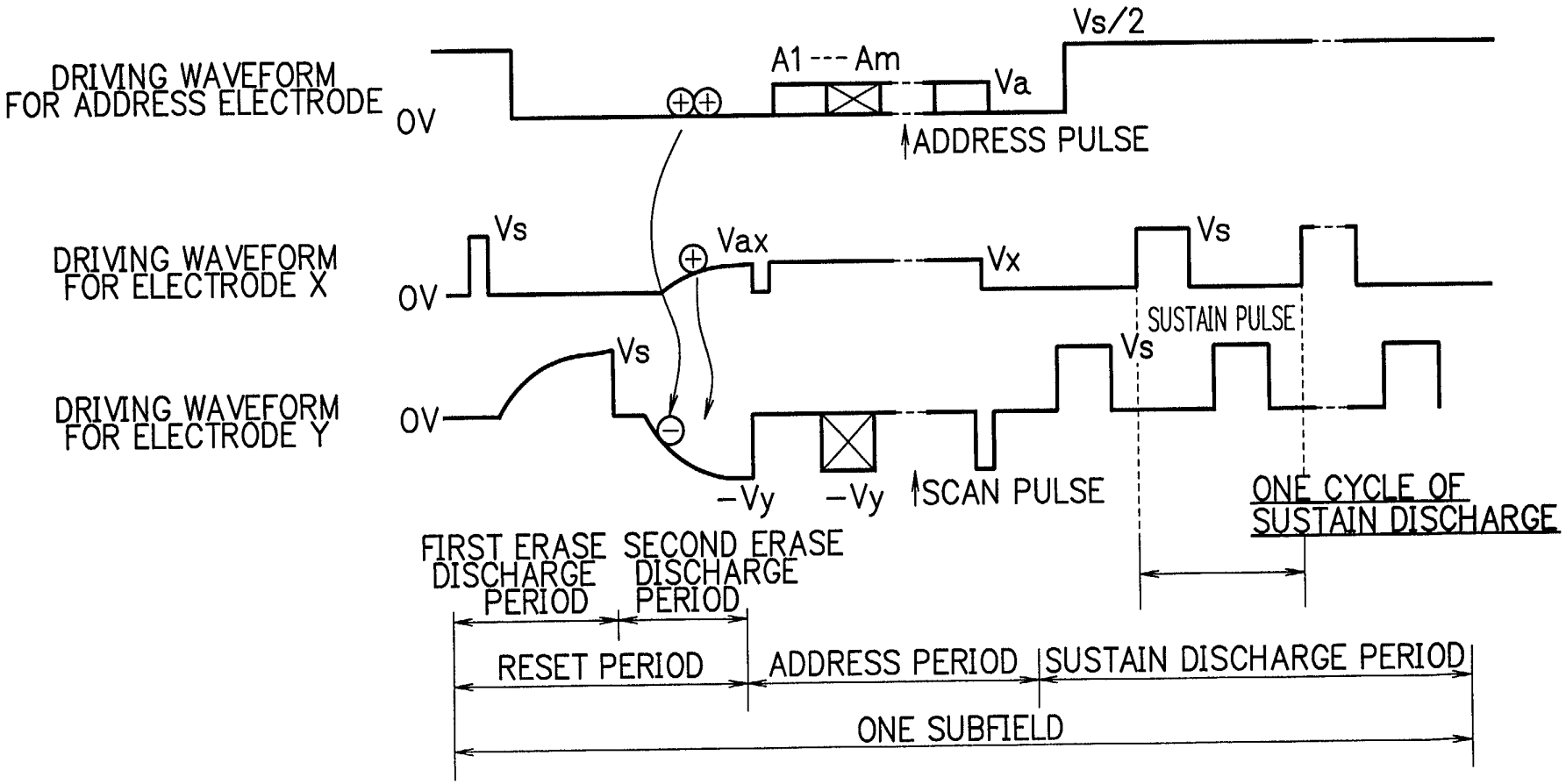


ILLUSTRATION FOR VARIABLE Vax

FIG. 10A

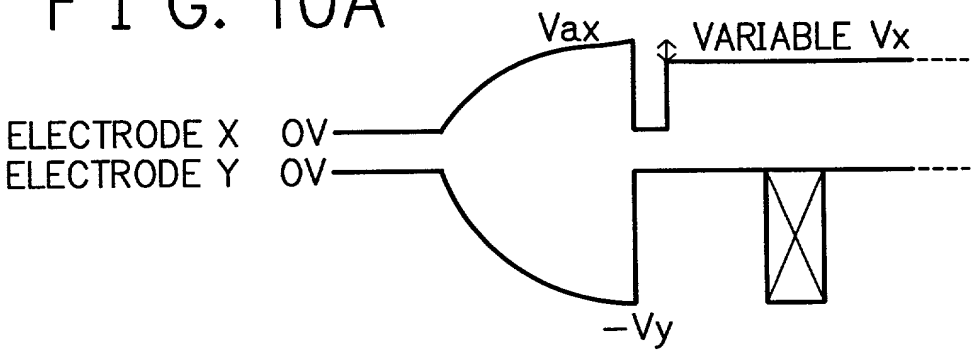


FIG. 10B

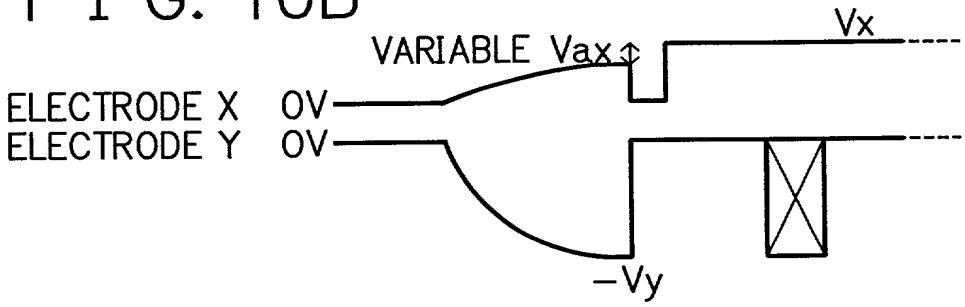
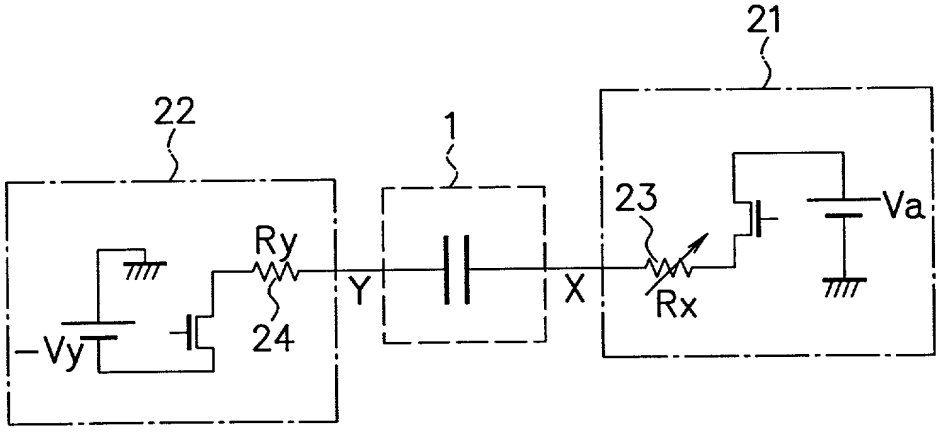


FIG. 11

HARDWARE ARRANGEMENT FOR VARIABLE Vax



CHARGE ACCUMULATION STATE IN EMBODIMENT

FIG. 12A

<END OF SUSTAIN>

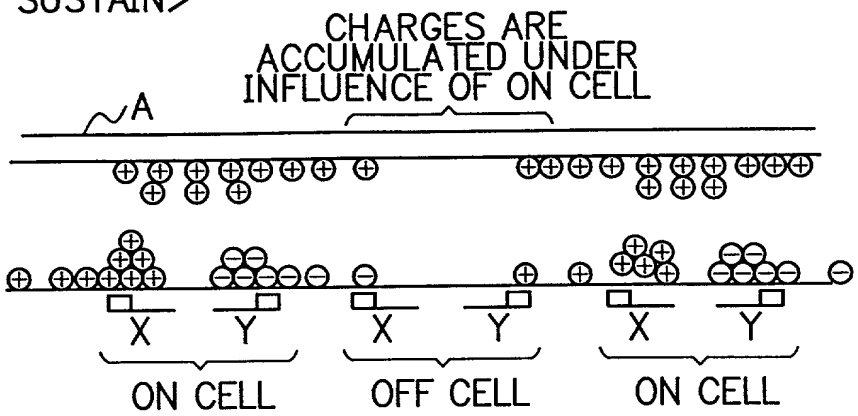


FIG. 12B

<ERASE>

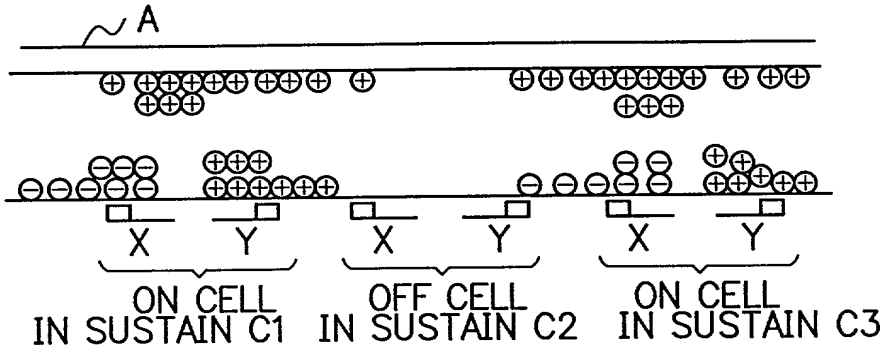


FIG. 12C

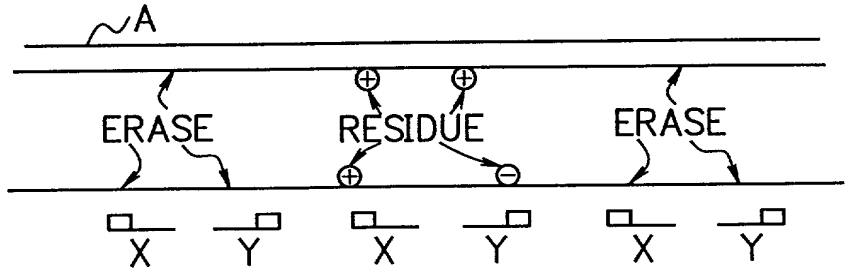


FIG. 12D

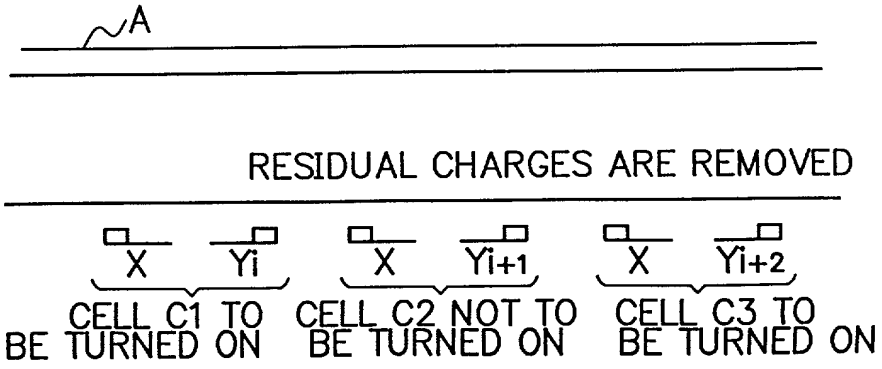


FIG. 13

ANOTHER EXAMPLE OF PDP DRIVING WAVEFORM

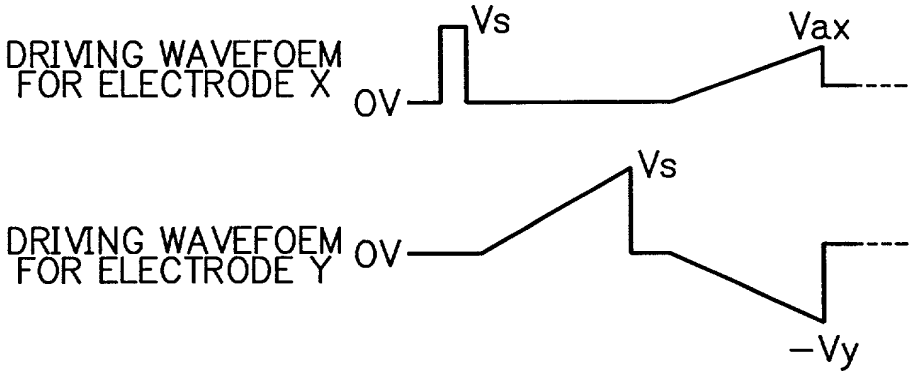
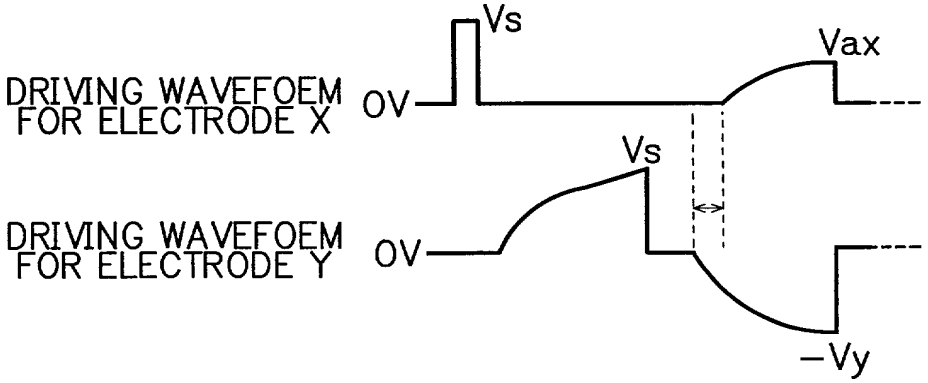


FIG. 14

ANOTHER EXAMPLE OF RISE TIMING OF SECOND POSITIVE OBTUSE WAVE



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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PLASMA DISPLAY DRIVING METHOD AND APPARATUS

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11-113773	Japan	April 21, 1999	☐
			☐

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I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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国籍		Citizenship Japan
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第二共同発明者	日付	Second inventor's signature Kouichirou Uchiyama Date Oct. 25, 1999
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国籍		Citizenship Japan
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(Supply similar information and signature for third and subsequent joint inventors.)

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国　籍		Citizenship Japan
私書箱		Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588 Japan
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第四共同発明者	日付	Fourth inventor's signature Date Takahiro Takamori Oct. 25, 1999
住　所		Residence Kawasaki-shi, Kanagawa Japan
国　籍		Citizenship Japan
私書箱		Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588 Japan

第五共同発明者		Full name of fifth joint inventor, if any
第五共同発明者	日付	Fifth inventor's signature Date
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国　籍		Citizenship
私書箱		Post Office Address
第六共同発明者		Full name of sixth joint inventor, if any
第六共同発明者	日付	Sixth inventor's signature Date
住　所		Residence
国　籍		Citizenship
私書箱		Post Office Address

（第七以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for seventh and subsequent joint inventors.)